We claim:

1. A method for one of reading a state from a ferroelectric transistor and storing a state in the ferroelectric transistor, the method which comprises:

providing, in a memory matrix, a memory cell with a ferroelectric transistor and further memory cells with further ferroelectric transistors;

one of reading a state from the ferroelectric transistor and storing a state in the ferroelectric transistor; and

increasing a threshold voltage of at least one of the further ferroelectric transistors in the memory matrix.

2. The method according to claim 1, which comprises reading the state from the ferroelectric transistor by applying a read voltage to a gate electrode of the ferroelectric transistor.

3. The method according to claim 1, which comprises storing the state in the ferroelectric transistor by applying a store voltage to a gate electrode of the ferroelectric transistor.

4. The method according to claim 1, which comprises increasing the threshold voltage of the at least one of the further ferroelectric transistors in the memory matrix by applying a

drain-substrate voltage to the at least one of the further ferroelectric transistors in the memory matrix.

5. The method according to claim 1, which comprises using a plurality of transistors in at least one of the memory cells.

6. The method according to claim 4, which comprises using, as the drain-substrate voltage, a voltage of substantially +3.3 volts.

7. The method according to claim 4, which comprises using, as the drain-substrate voltage, a voltage of substantially -3.3 volts.

8. A memory configuration, comprising:

a memory matrix including a plurality of memory cells connected to one another, said memory cells including ferroelectric transistors such that at least some of said memory cells each include at least a respective one of said ferroelectric transistors;

a read/store control apparatus connected to said memory cells for controlling one of reading a state from one of said ferroelectric transistors and storing a state to said one of said ferroelectric transistors; and

said read/store control apparatus being configured such that the state is one of read from said one of said ferroelectric transistors and stored in said one of said ferroelectric transistors, and such that a threshold voltage of at least a further one of said ferroelectric transistors in said memory matrix is increased.

9. The memory configuration according to claim 8, wherein:

said one of said ferroelectric transistors has a gate electrode; and

said read/store control apparatus is configured such that a read voltage is applied to said gate electrode for reading the state from said one of said ferroelectric transistors.

10. The memory configuration according to claim 8, wherein:

said one of said ferroelectric transistors has a gate electrode; and

said read/store control apparatus is configured such that a store voltage is applied to said gate electrode for storing the state in said one of said ferroelectric transistors.